B.Sc. PHYSICS LAB MANUAL

4th Semester

Prepared By

Pure & Applied Sciences

Physics

MIDNAPORE CITY COLLEGE

Course No: C10P:Analog Systems and Applications Lab

Credit: 2

Experiment-1

AIM: To study V-I characteristics of P-N junction diode, and Light emitting diode.

Apparatus:

1. Regulated Power Supply(0 – 30 V) DC
2. Digital Ammeter0-200µA/20mA
3. Digital Voltmeter 0-2V/20V DC
4. Bread board
5. Single strand connecting wires
6. Diode: IN4007
7. Resistor: 1 kΩ, 10 kΩ

Theory:

A p-type semiconductor in contact with an n-type semiconductor constitutes a p-n junction. p-n junction is a p-n diode which permits the easy flow of current in one direction but restrains the flow in opposite direction.

In forward bias condition, the positive terminal of the battery is connected to the p-side of the diode and negative terminal to the n side. In forward bias, when the applied voltage is increased from zero, hardly any current flows through the diode in the beginning. It is so because the external voltage is being opposed by the barrier voltage (VB)whose value is 0.7 volts for silicon and 0.3 volts for germanium. As soon as VB is neutralized, current through the diode increases rapidly with increase of applied voltage. Here, the current is in the order of mA.

When the diode is in reverse bias, the majority carriers are blocked, and only a small current due to minority carriers flows through the diode. As the reverse voltage is increased from zero, the reverse current increases and reaches a maximum saturation value Io, which is also known as reverse saturation current. This is in the order of nA for silicon and µA for germanium.

The current I flowing through the diode is related to the applied voltage by the following equation whether the diode is in forward bias or in reverse bias.

$$I = I_0(e^{V/\eta v_T} - 1)$$

Where,
I_0= Reverse saturation current.
V = Voltage applied to the diode

I = Current flowing in the diode
η = 1 for Ge and 2 for Si
V_T = Volt-equivalent of temperature=kT/q=T/11,600=26mV (@ room temp).

Circuit Diagram:

i.) For forward bias:

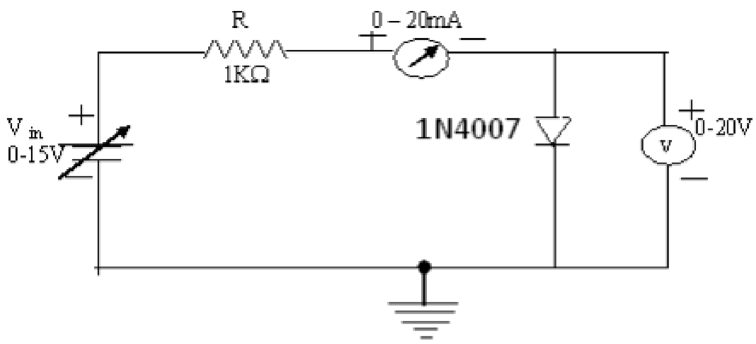


Fig. 1: Forward bias of P-N Junction diode.

ii.) Reverse bias:

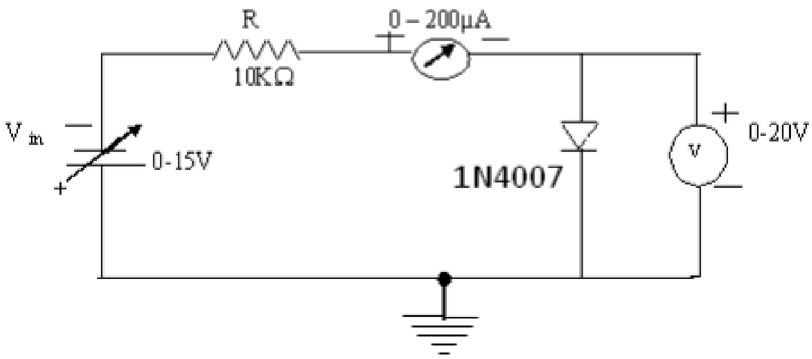


Fig. 3: Reverse bias of P-N Junction diode.

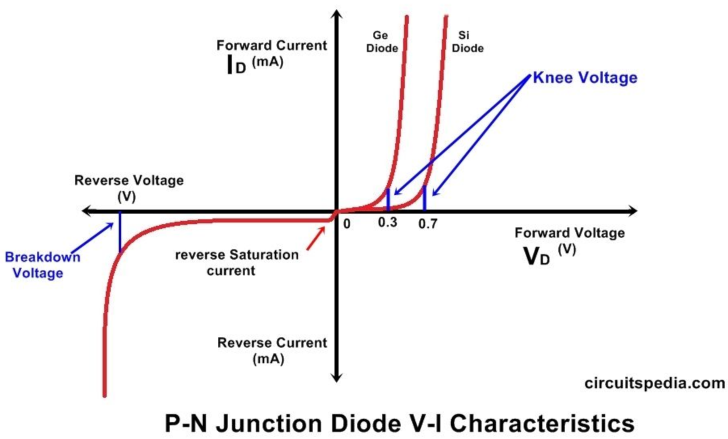


Fig. 4: P-N Junction Diode V-I Characteristics.

Procedure:

Forward Bias Condition:

1. Connect the circuit as shown in figure (1) using silicon PN Junction diode.
2. Vary Vf gradually in steps of 0.1 volts upto 5volts and note down the corresponding readings of I_f .
3. Step Size is not fixed because of non-linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
4. Tabulate different forward currents obtained for different forward voltages.

Reverse bias condition

1. Connect the circuit as shown in figure (2) using silicon PN Junction diode.
2. Vary Vr gradually in steps of 0.5 volts upto 8 volts and note down the corresponding readings of Ir.
3. Tabulate different reverse currents obtained for different reverse voltages. (Ir = VR / R, where VR is the Voltage across 10KΩ Resistor).

Observation:

Si diode in forward biased conditions:

Table 1: Forward Biased

Sl. No	RPS Voltage	Forward Voltage across the diode V_f (volts)	Forward current through the diode I_f (mA)

Si diode in reverse biased conditions:

Table 2: Reverse Biased

Sl. No	RPS Voltage	Reverse Voltage across the diode V_r (volts)	Reverse current through the diode I_r (μA)

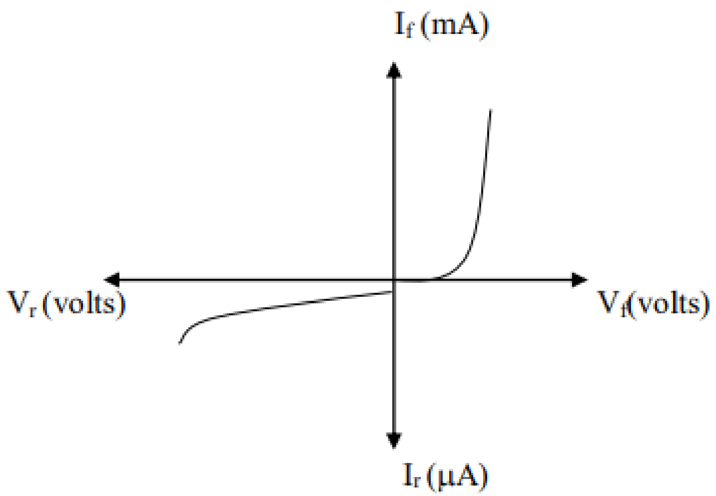
Graph (Instructions):

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark

 + ve x-axis as Vf
 - Ve x-axis as Vr
 + Ve y-axis as I_f
 - Ve y-axis as Ir.

3. Mark the readings tabulated for Si forward biased condition in first Quadrant and Si reverse biased condition in third Quadrant.

Calculations from Graph:



Static forward Resistance Rdc = V f / If Ω

Dynamic forward Resistance r ac = ΔV f /ΔIf Ω

Static Reverse Resistance $R_{dc} = V_r / I_r$ Ω
Dynamic Reverse Resistance $r_{ac} = \Delta V_r / \Delta I_r$ Ω

Result:

1. Cut in voltage = ……… V
2. Static forward resistance = ………. Ω
3. Dynamic forward resistance = ………. Ω

Precaution:

1. Maximum forward current should not exceed the value which is given in the datasheet. If the forward current in a pn junction is more than this rating, the junction will be destroyed due to overheating

2. Reverse voltage across the diode should not exceed peak inverse voltage (PIV). PIV is the max. reverse voltage that can be applied to a pn junction without any damage to the junction.

Conclusion:

Experiment-2

AIM: To study the V-I characteristics of a Zener diode and its use as voltage regulator.

Apparatus:

1. Bread Board
2. Connecting wires
3. Volt meter (0 - 20V)
4. Ammeter (0 - 20 mA), (0 – 20mA)
5. Regulator DC power supply
6. Zener diode (IN 2804)
7. Resistor (1kΩ)

Theory:

An ideal P-N Junction diode does not conduct in reverse biased condition. A zener diode Conducts excellently even in reverse biased condition. These diodes operate at a precise Value of voltage called break down voltage. A zener diode when forward biased behaves like an ordinary P-N junction diode. A zener diode when reverse biased can either undergo avalanche break down or zener break down.

Avalanche break down:-If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction may Name QtyZener Diode Resistor 1KΩ 1 1 rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in avalanche multiplication.

Zener breaks down:-If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces. Application of even a small voltage at the junction ruptures covalent bonding and generates large number of charge carriers. Such sudden increase in the number of charge carriers results in zener mechanism.

Circuit:

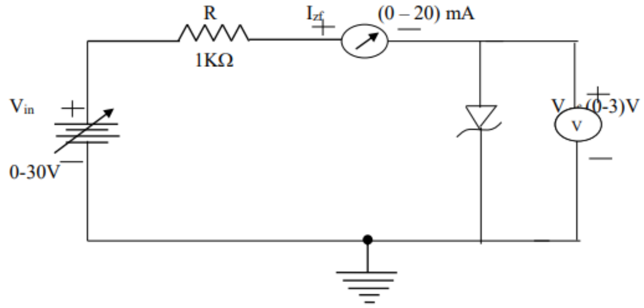


Fig. 1: Forward Bias Condition

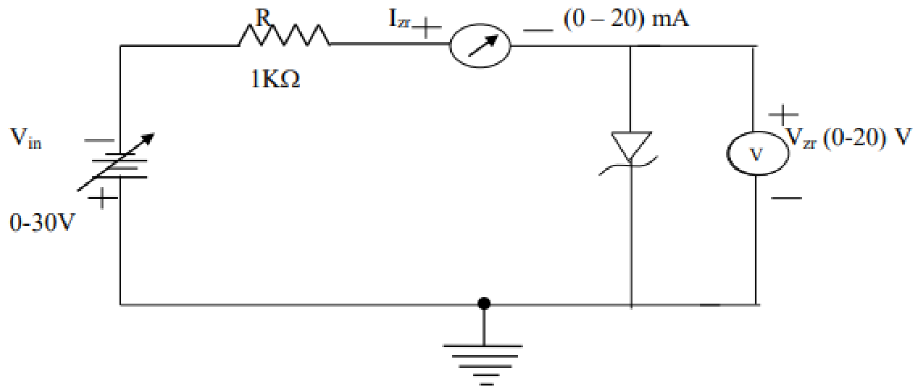


Fig. 2: Reverse Bias Condition:

Procedure:

Forward Bias:

1. Connect the circuit as per the circuit diagram figure 1.
2. The DC power supply is increased gradually in steps of 0.1 voltupto 5V.
3. Corresponding Voltmeter and Ammeter readings are noted and the V-I characteristics are plotted with zener voltage on X axis and current along the Y axis.
4. Break voltage is found and the break down resistance of zener diode is calculated.

Reverse Bias:

1. Connect the circuit as per the circuit diagram figure 2.
2. The DC power supply is increased gradually in steps of 0.2 voltupto 10V.
3. Corresponding Voltmeter and Ammeter readings are noted and the V-I characteristics are plotted with zener voltage on X axis and current along the Y axis.
4. Break voltage is found and the break down resistance of zener diode is calculated

Observation Table:

Forward bias **Table-1**

Sl.No	RPS Voltage	Forward Voltage across the diode V_{zf} (volts)	Forward current through the diode I_{zf} (mA)

Reverse bias **Table-2**

Sl.No	RPS Voltage	Reverse Voltage across the diode V_{zr} (volts)	Reverse current through the diode I_{zr} (mA)

Graph Instructions:

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.

2. Now mark

+Ve x-axis as V_{zf}

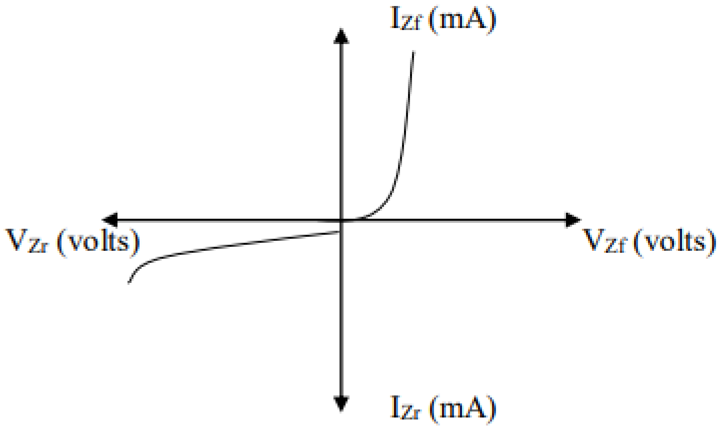
-Ve x-axis as V_{zr}

+Ve y-axis as I_{zf}

-Ve y-axis as I_{zr}

3. Mark the readings tabulated for zener diode forward biased condition in first Quadrant and Zener diodes reverse biased condition in third Quadrant.

Calculations from Graph:



Static forward Resistance Rdc = Vzf/Izf
Dynamic forward Resistance rac = ΔVzf /ΔIzf
Static Reverse Resistance Rdc = Vzr / Izr
Dynamic Reverse Resistance rac = ΔVzr/ΔIzr

Result:

a. Zener Voltage = _______________
b. The zener resistance at the breakdown voltage was found to be = ...
c. Forward bias resistance =__________
d. Reverse bias resistance = __________

Precaution:

1. It is preferable to use digital Multimeter in place of analog voltmeter
2. Maximum current should not exceed the value which is given on the data sheet.

Conclusion:

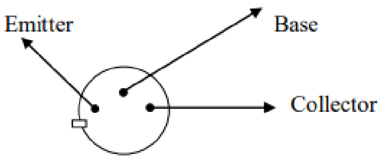
Experiment- 3

AIM: To study the characteristics of a Bipolar Junction Transistor in CE configuration.

Apparatus:

1. Dual Regulated power supply (0 – 30) V
2. Moving coil ammeter (0 – 10 mA), (0 -1mA)
3. Moving coil voltmeter (0 – 1 V), (0 – 10 V
4. Bread board – 1
5. Resistor- 220 K-ohm, 560ohm.
6. Transistor CL 100- 1
7. Connecting wires (single strand)

Pin Assignment of Transistor:



Theory:

In this CE arrangement, input is applied between base & emitter terminals and output is taken from collector and emitter terminals. Here emitter of the transistor is common to both input and output circuits. Hence the circuit name is Common Emitter (CE) configuration.

For CE configuration, we define the important parameters as follows:

1. The base current amplification factor (β) is the ratio of change in collector current ΔIC to the change in base current ΔIB is known as Base current amplification factor.

$$B = \Delta I_C / \Delta I_B \Big|_{VCB = \text{Constant}}$$

In almost any transistor, less than 5% of emitter current flows as the base current. The value ofβ is generally greater than 20.Usually its value ranges from 20 to 500. This type of arrangement or configuration is frequently used as it gives appreciable current gain as well as voltage gain.

2. Input resistance is the ratio of change in base-emitter voltage to the change in base-current at constant V_{CE} i.e.,

$$r_{i} = \Delta V_{BE} / \Delta I_B \Big| V_{CE=Const}$$

The value of input resistance for the CE circuit is of the order of a few hundredΩ's.

3. Output resistance is the ratio of change in collector-emitter voltage to change in collector current at constant I_B

$$r_0 = \Delta V_{ce}/\Delta I_C \big|_{I_E = \text{Constant.}}$$ (It is in the order of 50 kΩ)

Circuit Diagram:

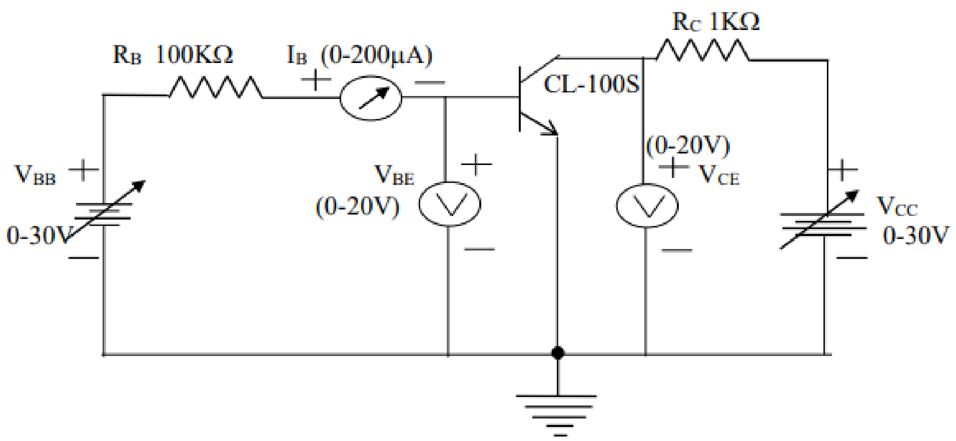


Fig. 1: For input characteristics of BJT.

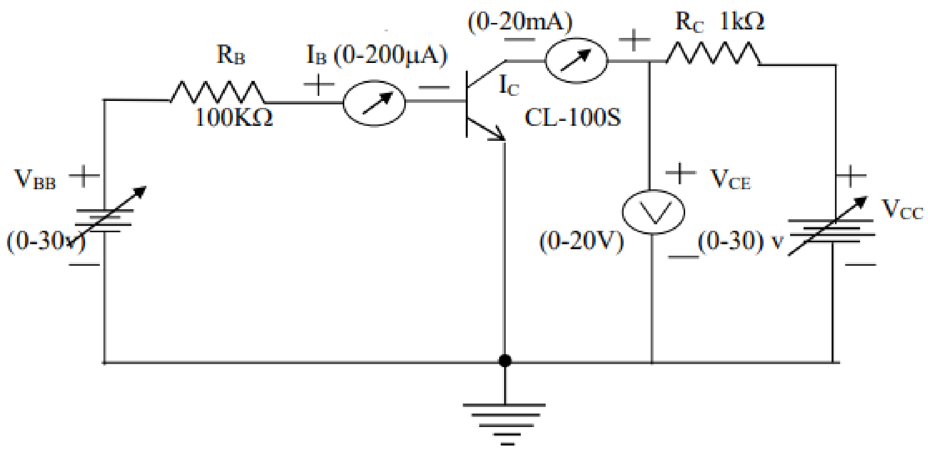


Fig. 2: For output characteristics of BJT.

Procedure:

Input characteristics:

1. Connect the circuit as per the given circuit diagram (Fig-1) on bread board
2. Set V_{CE} = 5V, vary V_{BE} in steps of 0.1V & note down the corresponding I_B. Repeat the above procedure for 10V, 15V & 20V
3. Plot the graph V_{BE}vs. I_B for a constant V_{CE} taking V_{BE} is taken on x-axis & I_B on y-axis

$$\Delta V_{BE}/\Delta I_B \big|_{V_{CE} = \text{Constant}}$$

4. Calculate input resistance

1. Connect the circuit as per the given circuit diagram on the bread board
2. Open the input circuit, vary the collector voltage V_{CE} in steps of 1V and note down the corresponding collector current I_C.
3. Set I_B= 20μA, vary V_{CE} in steps of 1V and note down the corresponding I_C. Repeat the above procedure for 40μA, 80μA, 100μA.
4. Plot the graph taking VCE on X-axis & IC on y-axis at corresponding constant IB
5. Calculate the output resistance

$\Delta V_{CE}/\Delta I_C \mid I_B$= Constant

6.Calculate the current amplification factor ,$\beta = \Delta I_C/\Delta I_B$

Observation Table:

Table 1: For Input Characteristics

I V_{CE} = 0 V		V_{CE} = 5 V	
I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)

Table 2: For Output Characteristics

I_B= 20μA		I_B = 40μA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

Expected Graph:

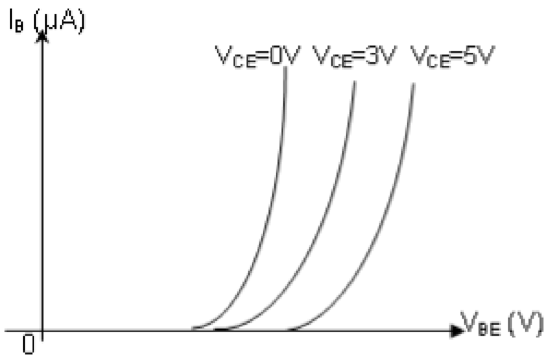


Fig 3: Input Characteristics

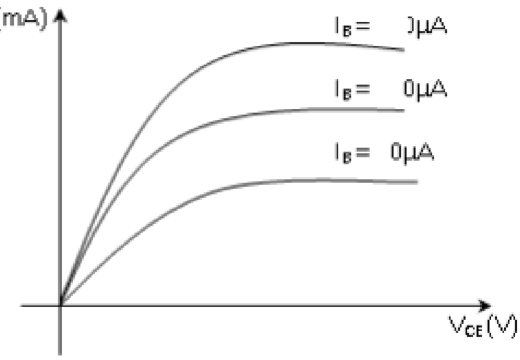


Fig 4: Output Characteristics

Calculation:

I/p Resistance= ΔVBE/ΔIB │VCE= Constant
O/p Resistance = ΔVCE/ΔIC │Ib= Constant
Current amplification factor=β= ΔIC/ΔIB

Precaution :

1. While doing the experiment do not exceed the ratings of the Transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
3. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

1. Input Resistance (Ri) = ……………Ω
2. Output Resistance (Ro) = ……………Ω
3. $\beta = I_c/I_B$ |Vce=constant ______

Conclusion:

Experiment-4

AIM: To study the various biasing configurations of BJT for normal class A operation.

Apparatus:

1. Transistor-CL100, BC558
2. Resistor-47k ,33 ,220Ω
3. Capacitor-47 µ F
4. Signal Generator-(0-3))MHz
5. CRO-30MHz
6. Regulated power supply-(0-30)V
7. Bread Board

Theory:

The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle. For all values of input signal, the transistor remains in the active region and never enters into saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally.The collector current is flows for 3600 (full cycle) of the input signal. i e the angle of the collector current flow is 3600.

Circuit Diagram:

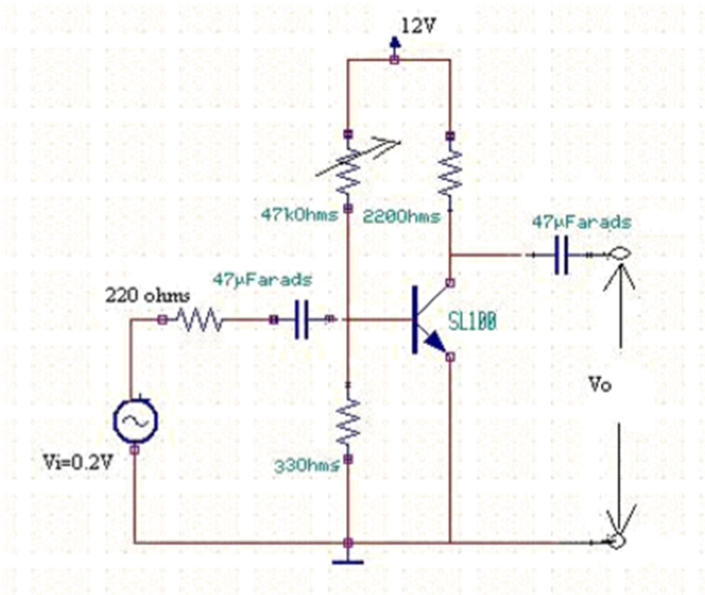


Fig1

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 10 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency(Hz).

Observation Table 1:

Keep the input voltage constant, Vin =

Frequency (in Hz)	**Output Voltage (in volts)**	**Gain = 20log (Vo/Vin) (in dB)**

Formula:

Maximum power transfer = $P_{Omax}=V^{2}/R_{OL}$
Efficiency η = Pomax/Pc

Result:

Thus the Class A power amplifier was constructed. The following parameters were calculated:
a) Maximum output power=
b) Efficiency=

Conclusion:

Experiment- 5

AIM: To study the frequency response of voltage gain of a RC-coupled transistor amplifier.

Apparatus:

1. cathode ray oscilloscope
2. Regulated power supply
3. function generator
4. bread board
5. connecting wires
6. . Resistors- 15k,15k,10k,10k,3.3k,220,220Ω
7. Transistor-BC107, BC107
8. Capacitors-10µf, 10µf, 10µf, 10µf, 10µf

Theory:

Whenever large amplification with very good impedance matching is required using an active device such as a transistor or a field effect transistor a single active device and its associated circuitry will not be able to cater to the needs. In such a case single stage amplifier is not sufficient and one requires more stages of amplification i.e., output of one stage is connected to the input of second stage of amplification circuit and the chain continues until the required characteristics of amplifier is achieved such an amplifier is called as multistage amplifier.In multistage amplifier, the output signal preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling different types of coupling can be employed. They are

1. RC coupling
2. Transformer coupling
3. Direct coupling

RC coupling is most popularly used type of coupling because it is cheap and provides excellent fidelity over a wide range of frequency .it is usually employed for voltage.

Procedure:

1) Connect the circuit as shown in the figure.
2) Apply 1Khz frequencyand 20mv Vp-p Sine wave from function generator..
3) Observe input and output Waveforms simultaneously on C.R.O
4) Change the frequency of input signal from 10HZ to 1MHZ in steps and note amplitudes of input and output Waveforms(input signal should be maintained constant).
5) Calculate Voltage gain (A) for each (in db) verses frequency.

Circuit Diagram:

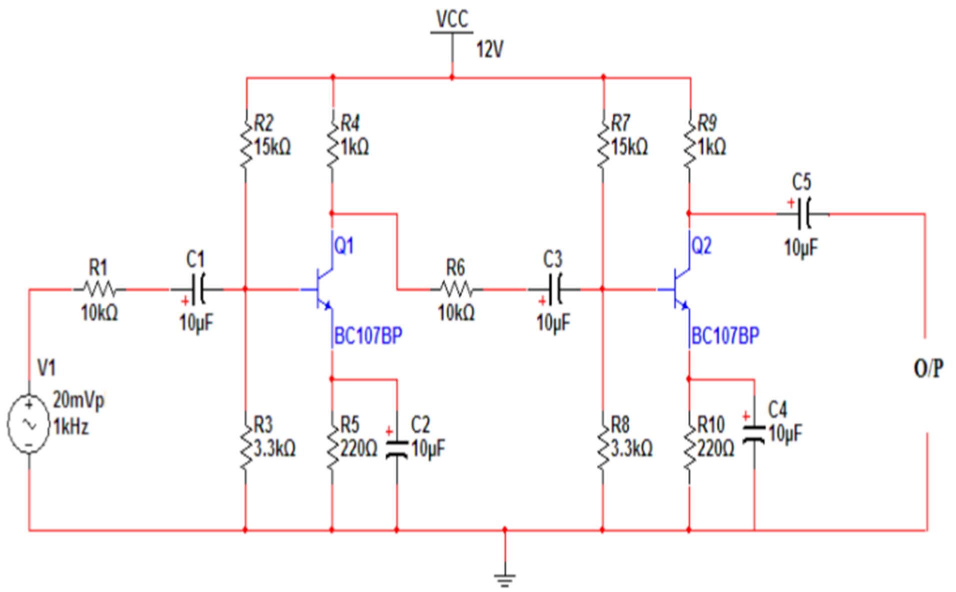


Fig 1: Two stage R-C Couple amplifier.

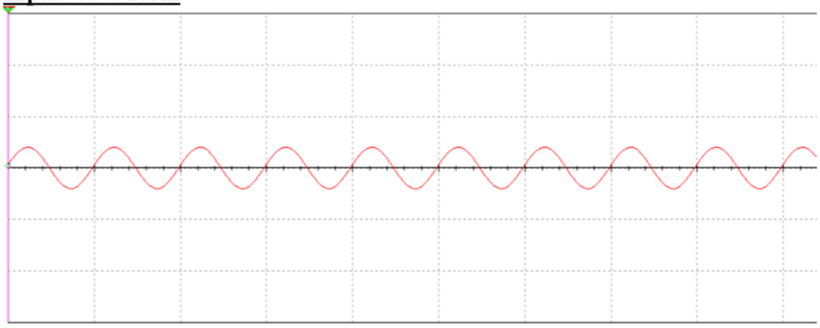
Observations:

Table -1

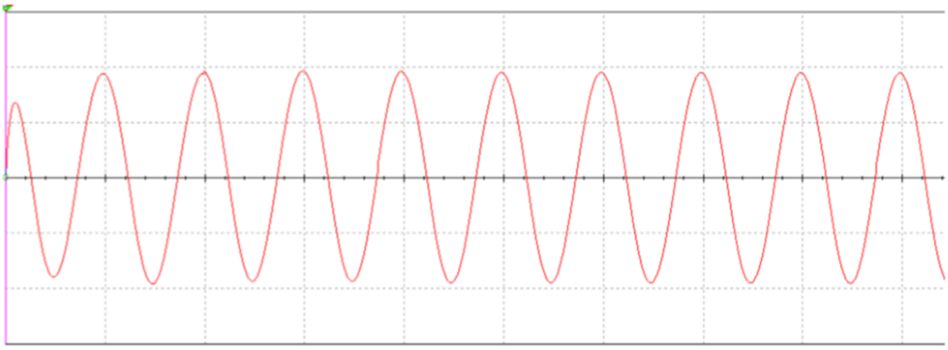
Sl. No.	Frequency Y (Hz)	Input Voltage (in Volts)	Output Voltage (in Volts)	Gain = Vo/Vin	Gain in dB= 20 log 10 (Vo/Vin)

Expected Graph:

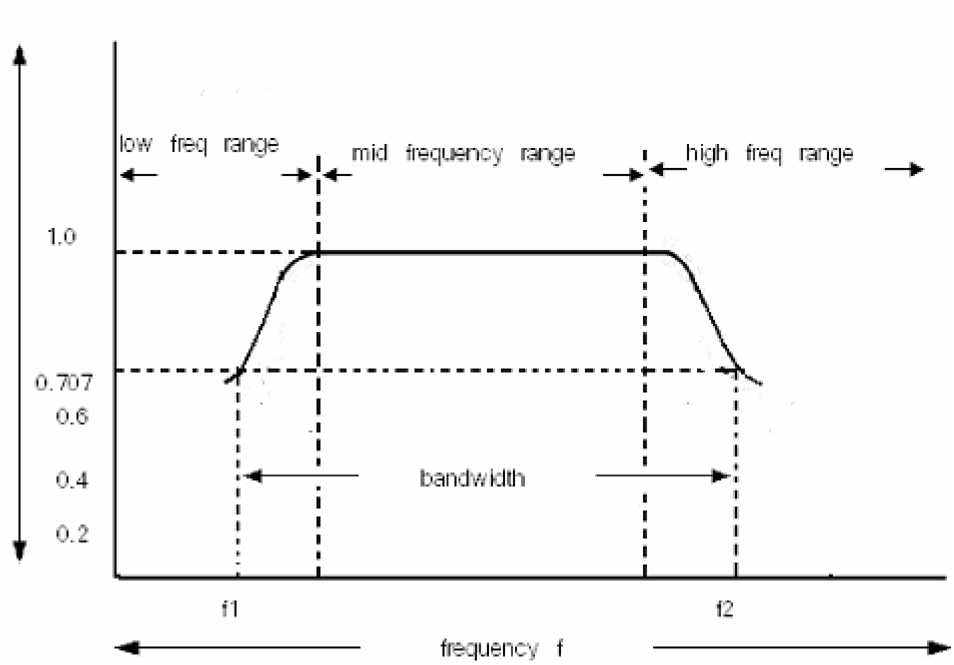
Input wave form



Output waveform



Frequency response:



Result:

1. Frequency response of two stage RC coupled amplifier is plotted.
2. Gain = _______dB (maximum).
3. Bandwidth= f_H--f_L = _________Hz. at stage 2.

Precaution:

1. Check connections before switching ON power supply.
2. Don't apply over voltage
3. When you are not using the equipment switch them Off

Conclusion:

Maximum gain of the amp:
Upper cutoff frequency f_2:
Lower cutoff frequency f_1:
Band width = f_2-f_1:

Experiment- 6

AIM: To design a Wien bridge oscillator for given frequency using an op-amp.

Apparatus:

1. Resistor- 10KΩ
2. Resistor- 3.3 KΩ
3. Function Generator-1MHz
4. I.C. 741 OP-AMP
5. CRO -20 MHz
6. Bread Board
7. Connecting Wires and Probes
8. Potentiometer-50 kΩ

Theory/Design:

Suppose we have to design oscillator of resonant frequency 965 Hz. We know that the resonant frequency f_0 is given by

$f_0 = 1/2\pi.R.C$

Let C = 0.05 μF therefore R will can be calculated as

R = 0.159 / {(965)0.05∗10^-6} = 3.3 kΩ

Let R_S= 10 kΩ

R_f= 2.Rs

Therefore R_f= 20 kΩ

Circuit Diagram:

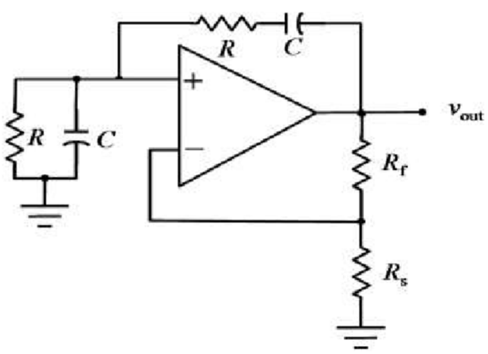


Fig 1: Wien Bridge Oscillator.

Procedure:

1. Connect the circuit as soon in figure and observe the output at pin number 6.
2. Trace it on CRO screen**.**

Observation:

Trace the waveform and measure the frequency and the verify .theoretical value with practical value.

Result:

Sinusoidal waveform was traced on pin 6 and verified with stated condition.

Conclusion:

Experiment- 7

AIM: To design a phase shift oscillator of given specifications using BJT.

Apparatus:

1. Transistor BC107
2. . Resistors: 10K (3Nos), 8KΩ or 10KΩ , 22KΩ , 1.2KΩ, 100KΩ
3. Capacitors: 0.001µf – 3 Nos
   10µF – 2Nos
   1µf -1
4. Regulated power Supply
5. CRO

Theory:

RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feedback Networks the output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequencies. Since CE Amplifier produces 180 º phases shift the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations.The frequency of oscillations of RC-Phase Shift Oscillator is,

$$f = 1/2\pi RC * \sqrt{6}$$

Circuit Diagram:

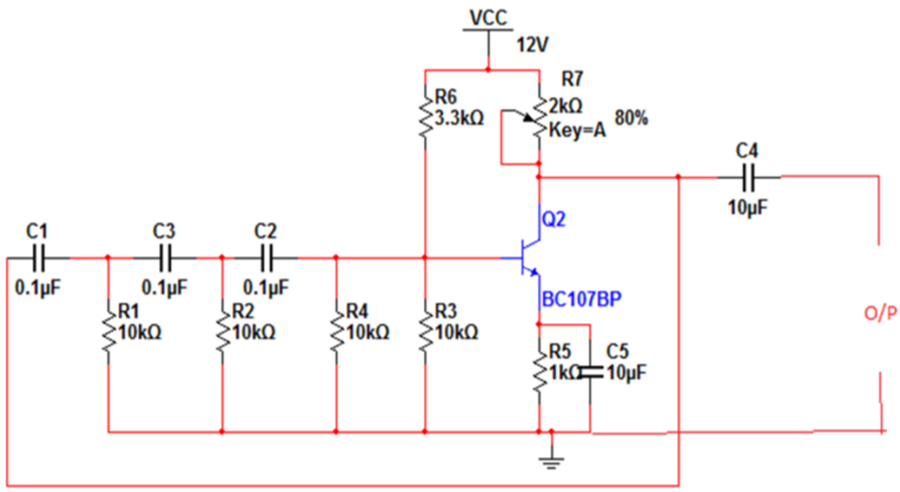


Fig. 1: Phase Shift Oscillator using BJT

Procedure:

1. Make the connection as per the circuit diagram as shown above figure 1.
2. Observe the output signal and note down the output amplitude and time period (Td).
3. Calculate the frequency of oscillations theoretically and verify it practically (f=1/Td).
4. Calculate the phase shift at each RC section by measuring the time shifts (Tp) between the final waveform and the waveform at that section by using the below formula.

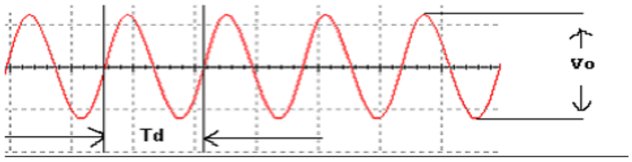
Observation:

Theoretical Calculations: R = 10KΩ, C = 0.001 μf

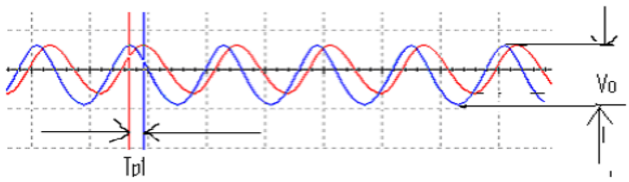
$$f = 1/2\pi RC * \sqrt{6}$$

Expected wave forms:

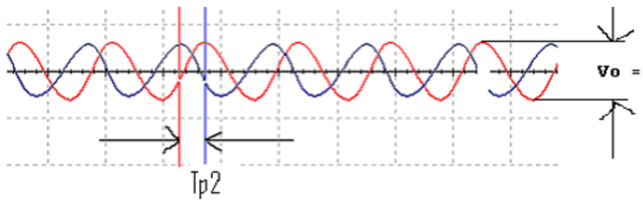
OUT PUT WAVE FORM :



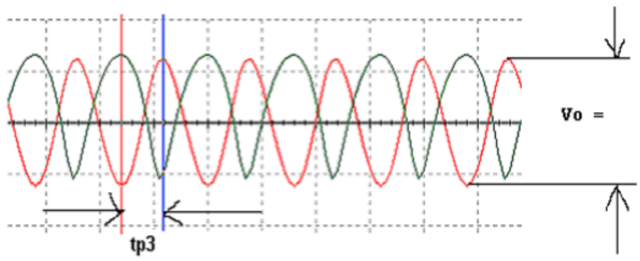
OUT PUT WAVE FORM : $\theta = 60^0$



OUT PUT WAVE FORM : $\theta = 120^0$



OUT PUT WAVE FORM : $\theta = 180$



Result:

The frequency of RC phase shift oscillator is calculated and the phase shift at different RC sections is noted.

Table- 1

Amplitude Voltage (V_{pp}) Volts	Time Period (ms)	Theoretical frequency (Hz)	Practical frequency (Hz)

Conclusion:

Experiment- 8

AIM: To design inverting amplifier using Op-amp (741,351) and study its frequency response

Apparatus:

1. Function Generator-1 KHz
2. CRO-20 MHz
3. Dual RPS-0 – 30 V
4. Op-Amp-IC 741
5. Resistors-R1= 100 Ω and RF= 1.5 K Ω

Theory:

The input signal Vin is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage Vo is fed back to the inverting input terminal through the Rf - R1 network, where Rf is the feedback resistor. The output voltage is given as,

$$V_0 = -R_f/R_1 \times Vin = -A_{CL}.Vin$$

Here the negative sign indicates that the output voltage is 180^0output of phase with the input signal.

Procedure:

1. Connections are given as per the circuit diagram.
2. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

Circuit Diagram:

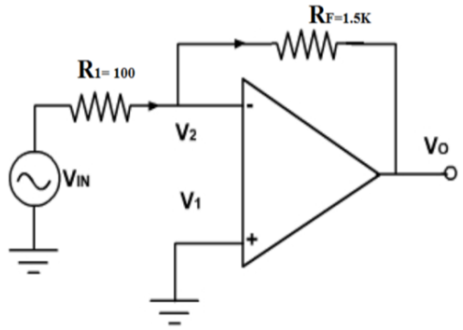


Fig. 1: Inverting Amplifier

Design:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$. Assume R_1 (approx. 100 Ω) and find R_F
Hence $V_o = - A_{CL} .V_{in}$

Observation:

Table -1: Observation Table of Inverting Amplifier

Sl no.	Input	Output	
		Practical	Theoretical
1	**Amplitude** **(No. of div ×Volts per div) in Volts**		
2.	**Time Period** **(No of div ×Time per div) in sec.**		

Result:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

Conclusion:

Experiment-9

AIM: To design summing amplifier using Op-amp (741,351) & study its frequency response

Apparatus:

1. Function Generator-3 MHz
2. CRO-30 MHz
3. Dual RPS-0 – 30 V
4. Op-Amp-IC 741
5. DC voltage source-12 V and 5 V
6. Resistors-R1= 10K Ω, R2= 47K Ω and RF= 10 K Ω

Theory:

Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non-inverting summer depending on the input applied to inverting & non-inverting terminals respectively. Circuit Diagram shows an inverting summing amplifier with 2 inputs. Here the output will be amplified version of the sum of the two input voltages with 180^0 phase reversal.

$$\text{Vout} = -\left[\frac{Rf}{R1}V1 + \frac{Rf}{R2}V2\right]$$

Procedure:

1. Check the components.
2. Setup the circuit on the breadboard and check the connections.
3. Switch on the power supply.
4. Give V1 = +12 V DC and V2 =+5V DC.
5. Observe the output voltage.
6. Repeat the procedure with V1 =1Vpp / 1 KHz sine wave and V2 = +1.5Vdc.
7. Make sure that the CRO selector is in the D.C. coupling position.
8. Observe input and output on two channels of the oscilloscope simultaneously.
9. Note down and draw the input and output waveforms on the graph.

Design:

The output voltage of an inverting summing amplifier is given by Vo = -(Rf / Ri).(V1+V2) .
Let R1 = 10 KΩ, R2 = 47 KΩ Then RF = 10 KΩ ,Then
$\text{Vout} = -[1V1 + 0.213V2]$

Circuit Diagram:

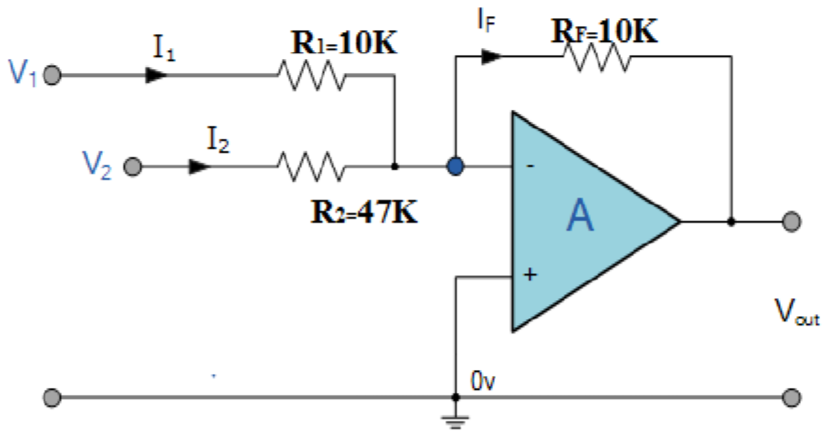


Fig 1: Summing Amplifier using OP-AMP

Observation:

V1= 12 DC, V2= 5 DC, Then Vo=? , V1 =1Vpp / 1 KHz sine wave and V2 = +1.5Vdc.

Then Vo=?.

Result:

Observe the input and output voltages on a Multimeter as well as CRO. Compare the experimental results with the theoretical value.

Conclusion: